

EAST SEARCH

8/16/05

		Databases	
L#	Hits	Search String	
S1	1254	((integrated or digital) near2 circuit\$1) with emulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	59	S1 and (distributed with (emulat\$3 or processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	6387	circuit\$1 with emulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
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S5	304	S2 or S4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	47	S5 and (reconfigurable with (logic or interconnect\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	127	S5 and (circuit with element\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	16	S5 and (circuit with partition\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	7	S5 and (on-board with processing\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	38	S5 and (element\$1 with state\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	67	S5 and ((monitor\$3 or report\$3 or test\$3) with request\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	48	S5 and ((monitor\$3 or report\$3 or test\$3) with command\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	27	S5 and (retriev\$3 with state\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	93	S5 and ((analyz\$3 or analysis) with data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	84	S5 and ((detect\$3 or report\$3) with event\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S16	87	S5 and (board with circuit\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S17	10	S5 and (on-chip with processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S18	54	S5 and (local\$2 with (monitor\$3 or analyz\$3 or analysis or report\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S19	30	S5 and (test\$3 with (vector\$1 or stimulus or stimuli))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	38	S5 and ((generat\$3 or produc\$3) with (vector\$1 or stimulus or stimuli))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S21	3	S5 and (local\$2 with (generat\$3 or produc\$3) with (vector\$1 or stimulus or stimuli))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
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S26	210	S7 or S14 or S15 or S16 or S23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	133	S25 and S26	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	167	S25 or S27	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	1254	((integrated or digital) near2 circuit\$1) with emulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S30	59	S29 and (distributed with (emulat\$3 or processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S31	6387	circuit\$1 with emulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S32	304	S31 and (distributed with (emulat\$3 or processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S33	304	S30 or S32	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S34	47	S33 and (reconfigurable with (logic or interconnect\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S35	127	S33 and (circuit with element\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S36	16	S33 and (circuit with partition\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

US 20040260530 A1	Distributed configuration of integrated circuits in an emulation system	20041223 703/23
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US 20040044514 A1	Polymorphic computational system and method in signals intelligence analysis	20040304 703/23
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US 20020116168 A1	METHOD AND SYSTEM FOR DESIGN VERIFICATION OF ELECTRONIC CIRCUITS	20020822 703/28
US 20020066065 A1	Method, apparatus, and program for multiple clock domain partitioning through retiming	20020530 716/6
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US 6732068 B2	Memory circuit for use in hardware emulation system	20040504 703/24
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US 6684318 B2	Intermediate-grain reconfigurable processing device	20040127 712/15
US 6571370 B2	Method and system for design verification of electronic circuits	20030527 716/4
US 6567962 B2	Method, apparatus, and program for multiple clock domain partitioning through retiming	20030520 716/6
US 6496918 B1	Intermediate-grain reconfigurable processing device	20021217 712/15
US 6415188 B1	Method and apparatus for multi-sensor processing	20020702 700/67
US 6377912 B1	Emulation system with time-multiplexed interconnect	20020423 703/28
US RE37488 E	Heuristic processor	20011225 706/14
US 6266760 B1	Intermediate-grain reconfigurable processing device	20010724 712/15
US 6052524 A	System and method for simulation of integrated hardware and software components	20000418 703/22
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US 5956518 A	Intermediate-grain reconfigurable processing device	19990921 712/15
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US 5838948 A	System and method for simulation of computer systems combining hardware and software inte	19981117 703/27
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US 5621651 A	Emulation devices, systems and methods with distributed control of test interfaces in clock don	19970415 703/23
US 5517597 A	Convolutional expert neural system (ConExNS)	19960514 706/26
US 5475793 A	Heuristic digital processor using non-linear transformation	19951212 706/14
US 5452239 A	Method of removing gated clocks from the clock nets of a netlist for timing sensitive implement	19950919 703/19

US 5377306 A	Heuristic processor	19941227 706/14
US 5357597 A	Convolutional expert neural system (ConExNS)	19941018 706/25
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US 5113500 A	Multiple cooperating and concurrently operating processors using individually dedicated memory	19920512 710/305
US 5087826 A	Multi-layer neural network employing multiplexed output neurons	19920211 706/38
US 4961002 A	Synapse cell employing dual gate transistor structure	19901002 365/185.03
US 4896053 A	Solitary wave circuit for neural network emulation	19900123 706/38
US 4802103 A	Brain learning and recognition emulation circuitry and method of recognizing events	19890131 706/38
US 4773024 A	Brain emulation circuit with reduced confusion	19880920 706/20